

ISSN : 2321-9602



Indo-American Journal of Agricultural and Veterinary Sciences



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DESIGN OF POWER-EFFICIENT TRUE SINGLE PHASE CLOCKING FLIP-FLOP USING 19 –TRANSISTOR BASED ON LOGIC STRUCTURE REDUCTION SCHEME

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Abstract: Flip flops are fundamental storage components employed widely in digital system designs, which apply intense pipelining methods and utilise numerous FF-rich modules, such as register files, shift registers, and FIFO, in order to store information. The power consumption of the FFs and clock distribution networks used in a typical digital system design There are just 19 transistors needed to create an ultralow-power, genuine single-phase clocking FF in this project. Master-slave logic is used in the design, which incorporates both static-CMOS and complementary pass-transistor logic. It is used to minimise the number of transistors needed to provide high power and delay performance in the design. Despite the circuit's simplicity, no internal nodes are allowed to float during operation in order to prevent power leakage. Improved time performance is achieved via a virtual VDD design method that speeds up state transitions in the slave latch. The power delay product is taken into account while designing transistors (PDP).

1. INTRODUCTION

Measures were done to lessen the burden on the clock system since flip flops use more power. In the past, a flip flop that had a smaller clock swing was used to reduce the clock's power. Clock systems voltage swing was decreased as a result of this technology [7]. Differential conditional capture flip flops employ a reduced swing approach to lower the clock burden; however, in this flip flop, the enable signal includes both low swing and full swing clock signals [6]. Flip flops such the differential discharge flip flop, differential pre-charge flip flop, pulse triggered flip flops, and so on were invented to minimise the circuit complexity since power was not lowered as planned. Using conditional capture and pre-charge approaches, flip flop switching

activity was reduced. Several factors are discussed in the work [8], including setup time, hold time, D-Q delay and C-Q delay.

Then, there's 2.

The most extensively used FF at the moment is a transmission-gate-based FF (TGFF). It's conceivable that the clock signal may be overworked when complementing signals are needed. As a result, even when data switching activity is modest, a significant amount of dynamic power is generated. To reduce clock signal burden, genuine single-phase clocking (TSPC) FF designs have recently been created. Circuits are often used to do this.

simplification. To facilitate single-clock-phase operations, cross-coupled set–reset (SR) latches replace the TG-based latch. There are a number of SR locks [12, 13] that are degenerate or topologically compressed [12, 13]. The SR-latch-based FF (SRFF) architecture is presented in this work, which incorporates both static-CMOS logic and complementary pass-transistor logic into a single design (CPL). In order to reduce the clock signal burden, this design adopts the TSPC operating concept. The design is optimised using both logic structure reduction and transistor optimization approaches.

The authors, H. Kawaguchi and T. Sakurai In order to save 63% of the power, an RCSF is used. The leak current cutoff technique is implemented in an unique flip-flop that is part of a reduced clock-swing flip-flop (RCSFF). VLSI clock system power consumption may be reduced by one-third using the RCSFF over the standard flip-flop. The decreased clock swing down to 1 volt results in this power gain. As a result, the RCSFF's area and latency may be lowered by a factor of around 20%. A lengthy RC interconnect's RC latency may be cut in half with the RCSFF.

As a result of this, RCSFF is recommended to reduce the clock system's voltage swing. Conventional flip-flop and suggested RCSFF schematic designs. It is impossible to lessen the clock swing with a normal flip-flop because and are necessary, and overhead becomes imminent if two clock lines and have to be distributed. On the other hand, if just is dispersed, most of the clock-related MOSFET's function at full swing, and very minimal power improvement is predicted. The RCSFF is made of a genuine single-phase master-latch and a cross-coupled NAND slave-latch. The master-latch is a current-latch-type sense-amplifier. The distinguishing characteristic of the RCSFF is that it can accommodate a decreased voltage swing owing to the single-phase nature of the flip-flop. The voltage swing, V_{clock} , may be as little as 1 V.

V. Oklobdzija, V. Stojanovic, D. Markovic, and N. Nedovic, Digital System Clocking High-Performance and Low-Power Aspects .

In CMOS multistage clock buffer architecture, the duty-cycle of clock is prone to be modified as the clock travels through numerous buffer stages. The pulse-width may be modified owing to imbalance of the p- and nMOS transistors in the long buffer. This article discusses a delay locked loop with double edge synchronisation for use in a clock alignment operation. Results of its SPICE simulation, that pertain to 1.2 μm CMOS technology, demonstrated that the duty-cycle of the multistage output pulses can be accurately set to (50 ± 1) percent within the operational frequency range, from 55 MHz up to 166 MHz. Almost all modern digital VLSI systems and other digital systems depend on clock pulses to govern the flow of data. To attain the greatest circuit speed in CMOS applications, the clock distribution system must be properly developed. A considerable lot of effort has been dedicated to clock recovery, clock regeneration, timing, and distribution throughout the previous few years.

B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia,

Improved sense-amplifier-based flip-flop design and measurements by J.K.S. Chiu and M. M.-T. Leung

A novel sense amplifier-based flip-flop (SAFF) is designed and experimentally evaluated. The output stage's cross-coupled set-reset (SR) latch was discovered to be the primary speed stumbling block in current SAFFs. A novel output stage latch architecture is used in the new flip-flop, which minimises latency and enhances driving capabilities greatly. Measurements on a test device developed in 0.18 μm effective channel length CMOS verify the flip-flop's performance. It is among the fastest flip-flops utilised in modern CPUs based on its demonstrated performance. The measuring set-up and methods used in this study are detailed in detail.

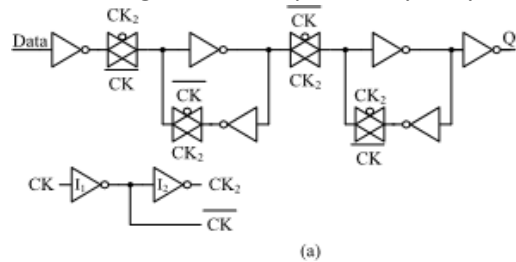
V. Stojanovic and V. G. Oklobdzija are the authors. Comparative study of high-performance and low-power master-slave latches and flip-flops. Consistently estimating the value of a variable is a challenge. Flip-flop and master-slave latch architectures have genuine performance and power characteristics. High performance as well as power budget constraints are the focus of a brand new model-based approach to simulation and optimization that is given. Performance and power consumption bottlenecks in various design types may be identified using the analytical method. In order to represent the actual qualities of the compared structures, several misleading parameters have been correctly adjusted and weighted. Our approach's benefits and the appropriateness of various design approaches for high-performance and low-power applications are shown by a comparison with sample master-slave latches and flipflops

COMPRESSED TOPOLOGICAL SCHEMES FOR 3LOW-POWE21-TRANSISTORS

3.2.1 Introduction

Logic for the Transmission Gates Transmission gates, like relays, may carry electricity.

Control signals with practically any voltage



potential may be used to either impede or impede both directions of movement. Unlike ordinary discrete field effect transistors, the substrate terminal (Bulk) is linked internally to the source terminal in a transmission gate made up of two field effect transistors. A n-channel MOSFET and a p-channel MOSFET are linked in parallel, but only the drain and source terminals of the two devices are connected. To create the control terminal, their gate terminals are linked together using a NOT gate (inverter).

This causes the N-channel MOSFET transistor to conduct and the transmission gate to conduct when one of the switching terminal voltages is increased towards the negative supply voltage (gate-source voltage). The n-channel MOSFET's gate-source voltage (also known as the gate-drain voltage) decreases when the voltage at one of the switching terminals of the transmission gate is increased to the positive supply voltage potential. The p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage), which causes this transistor to conduct and the transmission gate to switch. In this way, the transmission gate may travel throughout the whole voltage spectrum. When the voltage to be switched changes, the transmission gate's transition resistance changes as well, and this is because the resistance curves of the two transistors are superimposed

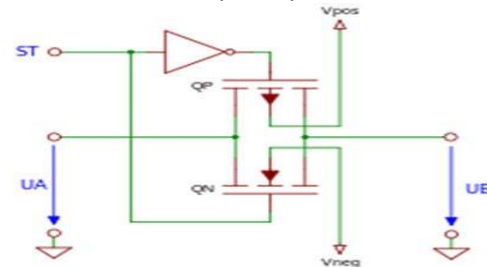


Fig1 Principle diagram of a transmission gate

Depending on the supply voltage and switching voltage, the control input ST must be able to control many logic levels. As a starting point, we'll look at some existing FF designs. Fig. 2 depicts a typical master-slave TGFF configuration

Fig2 Master Slave type TGFF

Indicating that there are two latch designs depending on TG. Inverters I1 and I2 are used to create clock signals with complimentary frequencies. With 12 transistors being driven by the clock, there is a large capacitive clock loading issue, and this design uses power even when the input is static. In typical SRFF designs, as illustrated in Fig.3, this issue is also present

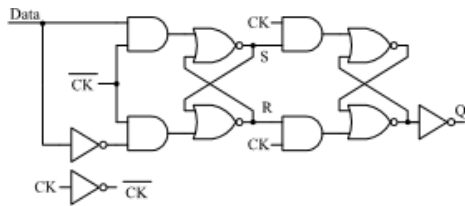


Fig3 Conventional SRFF designs

To overcome the power consumption problem, two FF designs employing an adaptive coupling (ac) technique and a topologically compressed scheme have been proposed. Fig. 4 shows the ac FF design .

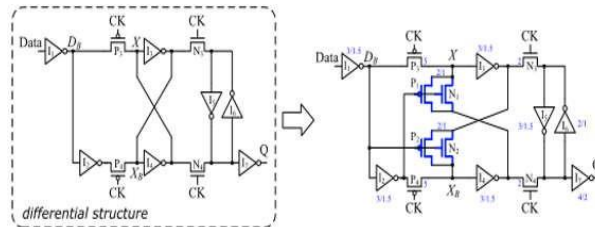


Fig4 AC Flipflop design

TSPC operation is achieved using a differential latch structure rather than the typical TGFF logic. n- or p-type pass transistors are used to replace the TGs. It is necessary to include level-restoring circuits into the master latch's cross-coupled channels in order to counteract any negative effects that process changes may have on the master latch. The clock signal drives just four MOS transistors in this configuration (two pMOS and two nMOS), reducing the transistor count to 22. Power consumption may be significantly reduced by reducing the clock burden and streamlining the FF circuit design. As the amount of data switching rises, the slave latch suffers from data contention, reducing the efficiency of this architecture. The master latch's level restoring circuit pair causes a longer setup time. When specific input and internal node combinations occur, this design has a power leakage issue.

3.2.1 Procedure

Topologically compressed FF (TCFF) is another TSPC FF designed on the foundation of an SR-latch and shown schematically in Fig.3.6. There is a logic diagram of this design in Fig. 3.5, and the original MOS circuit is depicted in Fig. 3.6. AOI gates, an inverter, and two AND-OR-Invert (AOI) gates form the core of the master latch, which operates as a MUX with feedback. When the clock signal CK is zero, the latch is transparent. Node x3's output is always the inverse of the input data because of the AOI gates and the inverter. Because the top AOI and the inverter form a closed route, the input data contribution is blocked and x3 stays unaltered when CK flips 1.

A pair of AOI gates and an inverter are also included in the slave latch. From the master's perspective,

Two AOI gates, controlled by the clock signal, feed latches to AND terms. This design uses just one phase of the clock signal. To improve the MOS circuit shown in the figure (3.6), the shared terms may be factored out. One CK-controlled nMOS transistor may be shared by both discharging routes in N (pull-down) logic. VDD is coupled to four pMOS transistors, two of which share the same inputs, in P logic. For the sake of efficiency, it is possible to remove two pMOS pairs from Master Latch.

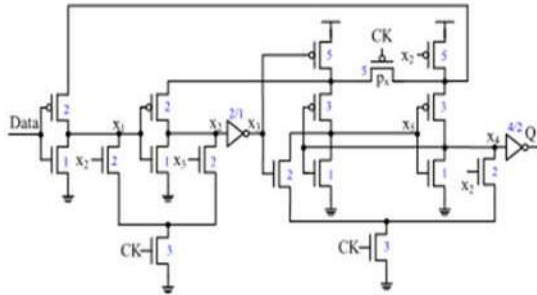
Furthermore, since the pMOS transistors on nodes x2 and x3 are always complementary, this implies that one of the two will always be ON. pMOS transistor's drain node is a virtual VDD when it is switched on. In order to eliminate the need for the two clock-driven pMOS transistors, an additional clock-controlled pMOS transistor may be added across the two AOI gates.

TPC 19-TRANSISTOR FLIP FLOP DESIGNED ACCORDING TO REDUCTIONSCHMES.

3.3.1 Introduction

The LRFF design may be seen as an improvement over the TCFF design in a variety of performance metrics.. Several optimization

techniques are used to obtain this look. To reduce setup time, the first approach is to



reduce logic, the second is to reduce circuit complexity, and third is to eliminate node floating to prevent the static power leak issue.

1 Flip-flop

There are two stable states in a flip-flop or latch that may be utilised to store state data. A flip-flop is a kind of vibrator that is both bi-stable and multi-vibrating. One or more control inputs and one or two outputs may be used to modify the circuit's state. In sequential logic, it is the fundamental storage element. Digital electronic systems, such as computers and communications, rely heavily on flip-flops and latches as basic building blocks.

ii) The Logic of the System

To begin with, it's important to have a clear understanding of the goals and indications you want to achieve.

They are used to categorise current and potential issues. Scenarios can be used to identify alternative futures

An alternate approach is to begin by identifying issues and verifying that all goals have been addressed. Possible instruments are then given as a means of overcoming the issues found.

In order to minimise the effect of the obstacles, strategies are devised as combinations of instruments.

A model may then be used to forecast the effects of the various instruments or techniques as a whole.

Afterward, the outcomes of these solutions are compared using an evaluation approach based on the goals.

In the course of this process, it's possible that new methods or tools may be developed.

As of right now, optimisation methods can be used to find better approaches.

An instrument or technique is chosen, and its performance is evaluated against the goals; these findings may assist improve future forecasts.

A monitoring programme evaluates the evolution of issues on a regular basis in light of the goals

Fig.5 Circuit optimization

Only three transistors are controlled directly by the clock signal, reducing the transistor count from 28 to 21. All of these aspects help the design save a lot of electricity. Even though the pull-up and pull-down logic networks have been much simplified, this design is completely static. TCF's design is built on the following three optimizations:

just one phased clock should be used

2) Reduce the clock's ability to control transistors Reduce the number of transistors in the system.

The TCF design's timing performance has been impaired despite a significant reduction in power consumption. To make matters even worse, the design relies on a poor pull-up network in which just two pMOS transistors are linked directly to the VDD. Three pMOS transistors in sequence form the critical route. Enlarging the pMOS transistors may help reduce this issue, but the power consumption will be increased as a result. VDD is coupled to four pMOS transistors, two of which share the same inputs, in P logic. Pass Transistor Logic Complementary

One pass transistor with CK as the control signal and x3 as the sink of the discharging current may be used to execute this phrase.

It is possible to create two different pathways for converging the discharge in the TCF design, each including one pass transistor.

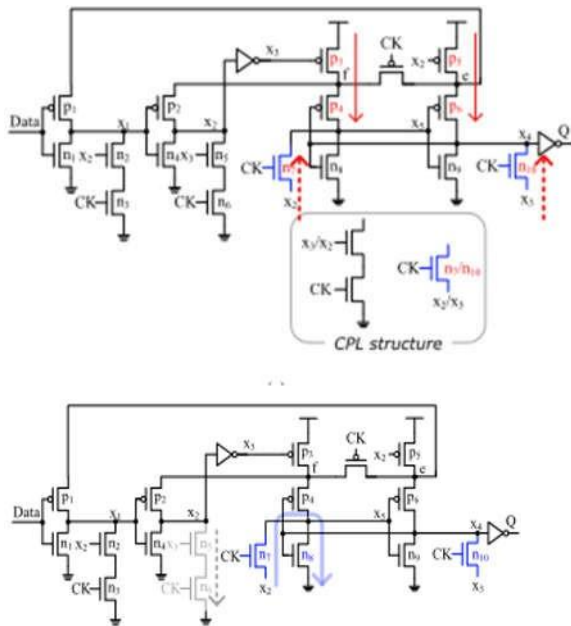
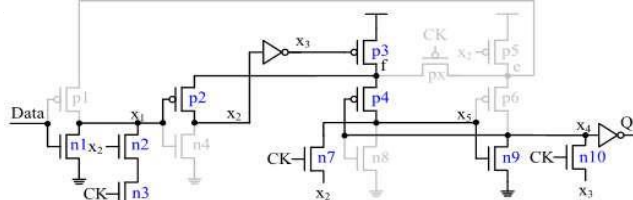


Fig.6 CPL Structure

As a result, the transistor count may be lowered by one since these two pass transistors work in a complimentary way. This logic structure reduction has two advantages. First and foremost, it streamlines the circuit to save electricity. It is possible that the pulldown delay will be somewhat longer than the worst-case time, but this is not the case (in contrast to the pull-up delay).

To begin with, when node x2 (or x3) is equal to 1, the pass transistor works in concert with the pull-up circuit established by pMOS transistor p3/p4 to raise the AOI output node to 1. This is the best route.

due to the ability to supply "weak 1" via pass transistors, it is regarded to be an accessory. However, when the slave latch is in the transparent mode (CK=1), this extra current increase improves the worst-case latency. It is possible to reduce the clock-to-Q (CQ) latency.



discharges only when both signals are equal to 1.

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Here we have a NOT-AND gate, which is just another way of saying, "And, then, not." If any of the inputs are low, the outputs of all NAND gates are high. And gate with little circle on the output is shown in the symbol. Inversion is shown by a tiny circle.

An OR gate followed by a NOT gate creates this kind of gate. If any of the inputs are high, the outputs of all NOR gates are low.s are low.

OR gate with little circle on the output is depicted by this symbol. Inversion is shown by a tiny circle.

Pass transistor n7 and pull-down transistor n8 are shown in Fig. 7.

Fig.7 New discharging from n7 and n8 to ground On the other hand, in an Active-low latch both inputs are normally HIGH, and the latch is triggered by a momentary LOW signal on either input. When the SET input momentarily goes LOW, the output goes HIGH. The output then stays HIGH until the RESET input momentarily goes LOW.

The master latch is in a transparent state, and nodes x2 and x3 are driven to 0 and 1, respectively. All transistors shown in gray are turned OFF. Signals from the master latch are blocked from entering the slave latch because both clockcontrolled feed-in transistors n7 and n10 are turned OFF. The slave latch is now in a hold state and the output remains unchanged.

Note that x2 and x3 fed to p3 and p5 of the slave latch are not for the purpose of signal input. Instead, they serve to control the pseudo VDD nodes e and f.

Fig.9Data latching process when ck=1,data=0 In order to assure that both nodes get VDD, the clock-controlled px connects them. The data

from the master latch (i.e., x2 and x3) are transferred to the slave latch via n7 and n10, respectively, when CK becomes 1, as shown in Fig. 3.21. x2 and x3 must keep their values for long enough to alter the slave latch's state (the hold time requirement). Node f is now isolated from VDD to promote a quick state change since the clock-controlled transistor px has been switched off.

If the input data changes after the hold period, both p2 and n4 are deactivated. The master latch is preventing the slave latch from receiving data from the master latch. Node x2 remains 0 due to the reverse signal flow via transistor n7. Consequently, there are no concerns with floating internal nodes in this way. They've deactivated all of the transistors shown in grey. Signals from the master latch cannot reach the slave latch because the clock-controlled feed-in transistors n7 and n10 are both turned OFF. The output from the slave latch has not changed. Process of latching data when ck=1 and data=1 (Fig.11)

Slave latches do not accept signals from external sources, such as the x2 and x3 wires provided to p3 and p5. Pseudo-VDD nodes E and F are in charge of controlling them. In order to assure that both nodes get VDD, the clock-controlled px connects them. When CK reaches the age of one. x2 and x3 must keep their values for long enough to alter the slave latch's state (the hold time requirement). Node f is now isolated from VDD to promote a quick state change since the clock-controlled transistor px has been switched off.

The master latch is transparent to new data and the slave latch retains its existing value in the situation of latching data=1, as shown in Figure 10. p3 is switched on and the bridge transistor px connects node f to node e, passing VDD via node f to node e. When data=0, this is the situation. If clock gating is used, we found a possible issue with internal node floating in the ACFF architecture during this assessment. When the clock signal was set to 1 and the input data changed from 1 to 0, the nodes X and XB in the circuit depicted in Figure 11 were found to be in a floating condition.

The waveforms of the simulation show that the levels of nodes X and XB degraded exponentially with each 1 to 0 transition of the input. It is possible to drift the values to 0.89 and 0.21 V, respectively, at a voltage of 1 volt for more than 200 ns, resulting in extra power usage.

Power-Delay-Product Evaluation

An overall composite performance indicator was used in our study. The suggested design's PDP and TCFF indices were the lowest when switching activity was 12.5%. The ACFF and TCFF indices were next lowest. The other four non-TSPC designs' indices, on the other hand, lagged far behind. The LRFF design, in particular, has the potential to achieve the finest possible balance between power and speed. Shows the PDP comparison findings under various switching operations in a bar chart. demonstrates how the PDP performs under 25 percent data switching probability process modifications. In order to get the best PDP number, the setup and hold times for each process corner (SS 0.8%/125°C, TT 1 V/25 °C, FF 1.2 V/40 °C, SF 1 V/25 °C, and FS 1 V/25 °C) were scoured. Process modifications were shown to have no effect on the performance of all FF design concepts. All the time, our design was ahead of the competition. Thus, the LRFF design's performance consistency has been confirmed by this test.

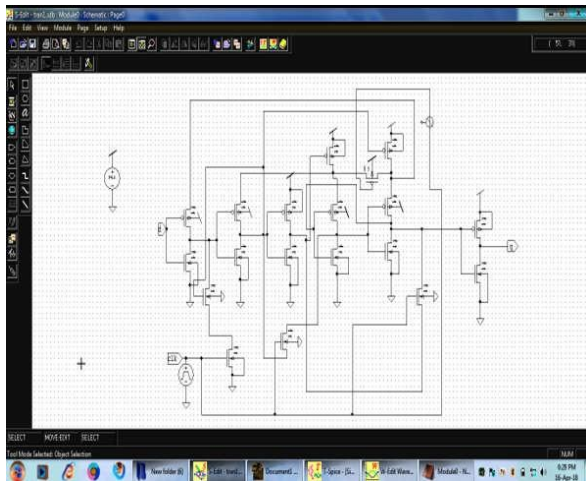
3.3.3 The Methodology

A MOS schematic shown in Fig. 3.8 illustrates that in the slave latch, the convergent discharging route controlled by the logic x2/x3 and CK is first separated into two independent discharging pathways, each including two nMOS transistors in series. If x2 is equal to 1 (or x3 is equal to 1), then x2 CK (or x3 CK) is logically identical. Because x2 and x3 are complimentary, $x2\text{ CK} = x3\text{ CK}$.

CK (or x3 CK Equals x2 CK) An implementation of this term may be done by utilising a single pass transistor with CK as the control signal and x3 as the sink of the discharging current, as shown in the little figure in Figure 3.14.

It is possible to create two different pathways for converging the discharge in the TCFF design, each including one pass transistor. As a result, the transistor count may be lowered by one

since these two pass transistors work in a



complimentary way. This logic structure reduction has a dual advantage. First, it reduces the circuit's power consumption. Although the pulldown delay may be a little longer than the worst-case time, it is not excessive (in contrast to the pull-up delay). As a second example, when node x2 (or x3) equals 1, the pass transistor works with the pull-up route established by pMOS transistors p3/p4 to raise the output of AOI to 1. Because a nMOS pass transistor may provide a "weak 1," this method is deemed auxiliary. It is only in the translucent mode (CK = 1) that this extra current increase improves the worst case latency. Clock-to-Q (CQ) latency may be a reduction in size is achieved. These two charging trajectories are shown in Fig. 3.14 by the dotted and solid arrowed lines (or x4). The second AOI gate of the master latch is reduced using the second logic structure reduction approach. It is only when CK and x3 are equal that the node x2 discharging route discharges. It is seen in Figure 3.18 that an additional avenue for discharging from node 2 is provided by pass transistor n7 in addition to n8 controlled by x4. We may now delete the original (and redundant) route from the circuit in order to make it easier to follow. Node x2's capacitive load is reduced while its power performance is improved. The master latch propagation latency may be reduced while running in the transparent mode, leading in a faster FF design setup time. Figure 3.19 depicts the circuit diagram after the implementation of the two logicstructure

reduction strategies. Only 19 transistors make up the whole circuit. In this case, just one phase of the clock is needed, and the fan-out for the clock signal is only four (one pMOS and three nMOS transistors). Static output node floating is avoided by using the suggested LRFF. Even if the design is not dynamic, the circuit complexity of its p-logic network is greatly decreased when CPL is used. The suggested design is able to simultaneously reduce circuit complexity and improve timing parameters.

RESULT AND ADVANTAGES

5.1 RESULT

Transistor count

- Transistor – 19

Power Results

- VVoltagesSource_1 from time 1e-008 to 4e-007
- Average power consumed-> 1.028366e-009 watts
- Max power 1.057001e-009 at time 1.02e-007
- Min power 9.382613e at time 1e-008

Propagation Time

- Paring 0.00 seconds
- Setup 0.00 seconds

- DC operating point 0.01 seconds
- Transient analysis 0.06 seconds

- Total 0.07 seconds

5.2 ADVANTAGES

- High speed
- Low power consumption and low voltage
- Low power dissipation
- Reduce circuit Area
- Reduce long discharging path problem

5.3 APPLICATIONS

- Used in low power applications
- Used in Memories
- Used in Sequential circuit
- Used in Chip designs

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CONCLUSION AND FUTURE SCOPE

5.4 CONCLUSION:

By modifying the SR latch structure and using hybrid logic of static-CMOS logic and CPL, we have developed a whole new FF architecture. An extra discharge channel between the master and slave latches shortens the transition time and improves power and speed performance, while also reducing circuit complexity. More than a few thousand simulations were run to examine key performance metrics including PDP and setup time delays as well as the CQ delays. The suggested design was found to be superior in almost every performance metric except for hold time. With regard to voltage and switching activity, the suggested design regularly beat the competition. This demonstrates that the suggested FF architecture is efficient.

FUTURE PERSPECTIVE

We are hopeful that the findings reported here will inspire more work on the TCFE approach. Sequential logic design and technology compatibility with TCFE are actively being investigated. The automation of logic design technique based on TCFE technology has received more attention lately..

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